Design and Digital Linearization of a High Efficiency Variable Conduction Angle Doherty Amplifier

By Sami Bousnina

> **The need for highly efficient, linear microwave power amplifiers has grown rapidly.**

Introduction

The need for highly efficient, linear microwave power amplifiers has grown rapidly, especially as mobile and satellite communication systems have been developed and expanded [1]. These systems employ multilevel digital modulation techniques to achieve higher-data-rate and multimedia services. This results in a band-limited multi-carrier signal, which is spectrally efficient but exhibits time-varying amplitude and phase characteristics. For acceptable linearity in handling such multi-carrier signals with high peak-to-average envelope ratios, the amplifier output power must be backed off from its peak value. This has the disadvantages of reducing amplifier efficiency, increasing energy consumption, and reducing the operating time of portable power sources. Such a tradeoff between linearity and efficiency is difficult to achieve with conventional amplifiers. One of the promising techniques for improving efficiency under output power backoff is the load-line modulation technique used in the Doherty amplifier [2]–[4]. A simplified basic block diagram of the Doherty amplifier is shown in Figure 1. Amplifier 1 is referred to as the *carrier* amplifier. Amplifier 2 is referred to as the *peak* amplifier. The input power is divided equally, with a quarter-wave delay at the input of the peak amplifier. After being amplified, the output signals are combined in phase at the output of the quarter-wave transformer (with characteristic impedance Zc).

Detailed analysis of the characteristics of the Doherty amplifier configurations based on *carrier* and *peak* amplifiers both biased in Class B is reported in [3]. In these configurations, an additional control circuit is needed to turn on the *peak* amplifier when the *carrier* amplifier saturates. Several designs of the Doherty amplifier [3]-[8] have reported non-constant gain and phase behavior, caused partially by the inherent nonlinearity in the *carrier* and *peak* amplifiers when biased in Class B (or AB) and Class C, respectively. Such nonlinearities of the AM-AM and AM-PM characteristics affect negatively the integrity of the transmitted signal and cause an increase
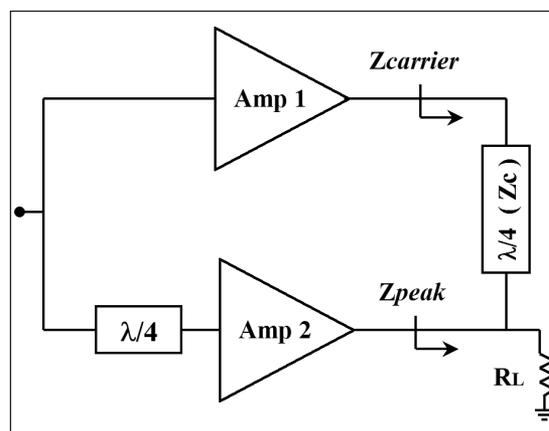

Figure 1 • Schematic of the Doherty amplifier.

in spectral re-growth. Linearization techniques applied to the Doherty amplifier offer a promising solution to improve its linearity over a wide input power range while maintaining high efficiency. A variety of linearization techniques have been reported in the literature [9]. The three main types are feedforward, feedback, and predistortion. The latter type has aroused increased interest during the past several years, mainly because of the availability of sophisticated digital signal processors.

In order to practically evaluate the merit of the Doherty amplifier in providing high efficiency under output power back-off, a design at 1.9 GHz of a Doherty amplifier configuration is presented. A digital predistorter is synthesized to rectify the nonlinearities of the designed amplifier without compromising its efficiency.

Theoretical Characteristics of the Doherty Amplifier Configurations

The principle of operation of the Doherty amplifier is better understood through its two stages of operation depending on the level of the input drive. In the first stage, the drive level is so low such that the *peak* amplifier remains off. Consequently, only the *carrier* amplifier amplifies the input signal (figure 2).

In the second stage, the drive level is high and exceeds certain threshold level allowing the *peak* amplifier to turn on. The bias of the *peak* amplifier in class C causes its conduction angle to vary with the level of the input drive. By varying the load seen by the *carrier* amplifier at low drive levels along with the threshold level of the input power that turns on the *peak* amplifier, different configurations of the Doherty amplifier can be distinguished. These configurations are also distinguished by the specific values of the load R_L of the overall Doherty amplifier and the characteristic impedance Z_C. The char-
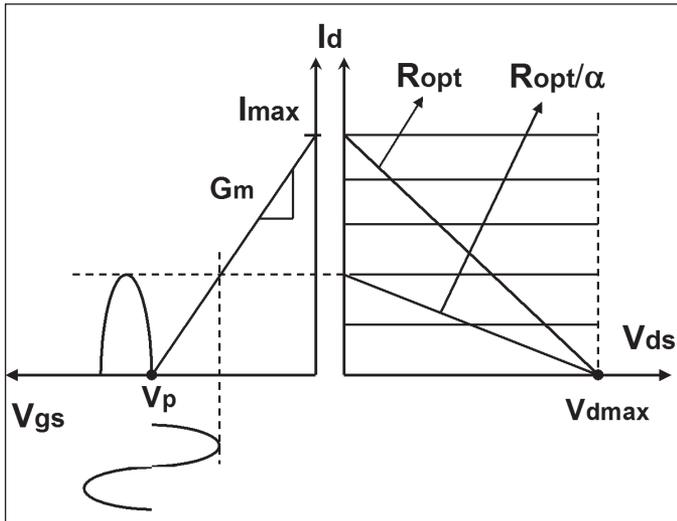

Figure 2 • Current and voltage waveforms and load-lines of the *carrier* amplifier.

acteristics of these configurations at maximum input drive level are defined by the following equations [4]:

The maximum conduction-angle of the drain current of the peak amplifier is defined by:

$$\theta_{max} = 2\cos^{-1}(\alpha) \qquad (1)$$

with $\quad \alpha = \dfrac{R_{opt}}{\left(Z_{carrier}\right)_{at\ low\ drive\ levels}} \qquad (2)$

The load of the Doherty amplifier, the impedance of the quarter-wave transformer, and the impedances presented to the *carrier* and *peak* amplifiers are defined by:

$$R_L = R_{opt}\ f(\alpha) \qquad (3)$$

With
$$f(\alpha) = \frac{2\beta + \alpha\beta^2 - \sqrt{\left(2\beta + \alpha\beta^2\right)^2 - 4\beta^2}}{2} \qquad (4)$$

and

$$\beta = \frac{\pi}{(1-\alpha)\left[\dfrac{\theta_{max} - \sin\theta_{max}}{1 - \cos\dfrac{\theta_{max}}{2}}\right]} \qquad (5)$$

and

$$Z_C = R_{opt}\sqrt{\frac{f(\alpha)}{\alpha}} \qquad (6)$$

$$Z_{carrier} = R_{opt}\sqrt{\frac{f(\alpha)}{\alpha}} \qquad (7)$$

$$Z_{peak} = R_{opt}\frac{f(\alpha)}{1 - \sqrt{\alpha\ f(\alpha)}} \qquad (8)$$

The output power back-off (insuring near peak efficiency), maximum output power and efficiency of the Doherty amplifier are defined by:

$$OPB = 10Log\left(\frac{1}{\alpha\ f(\alpha)}\right) \qquad (9)$$

$$P_{out\_max} = \frac{1}{8}\frac{V_{d\,max}^2}{R_{opt}\ f(\alpha)} \qquad (10)$$

$$\eta = \frac{1}{\dfrac{4}{\pi}\sqrt{\alpha\ f(\alpha)} + \dfrac{2(1-\alpha)}{\pi}f(\alpha)\left[\dfrac{2\sin\dfrac{\theta_{max}}{2} - \theta_{max}\cos\dfrac{\theta_{max}}{2}}{1 - \cos\dfrac{\theta_{max}}{2}}\right]} \qquad (11)$$
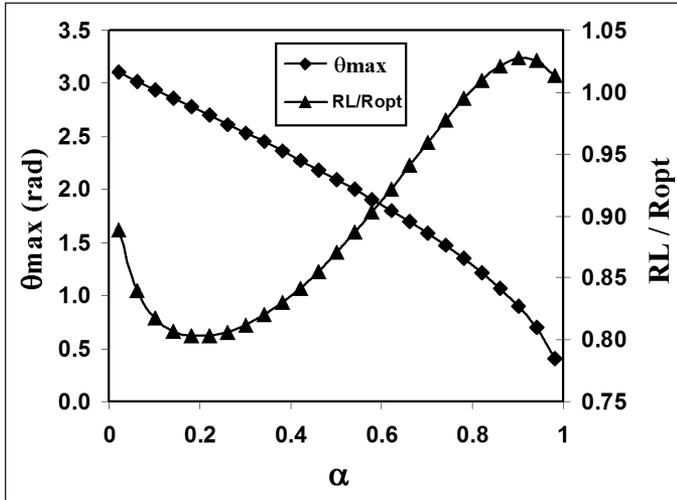
Figure 3 • Maximum conduction angle of the *peak* amplifier and normalized optimum loads for different configurations of the Doherty amplifier.

The variations versus α of the conduction angle of the *peak* amplifier at maximum input drive level and optimum load of the Doherty amplifier configurations are shown in figure 3.

Figure 4 shows the variation of the normalized impedances presented to the *carrier* and *peak* amplifiers at maximum drive level. At the extreme cases where $\alpha = 1$ or $\alpha = 0$ and as expected, theses impedances decrease to R_{opt} signifying that only the *peak* amplifier or the *carrier* amplifier operates whatever the level of the input drive. In addition, it can be concluded that while both the *carrier* and *peak* amplifiers are operating, the maximum output power is always lower than the double of the maximum power of the *carrier* amplifier.

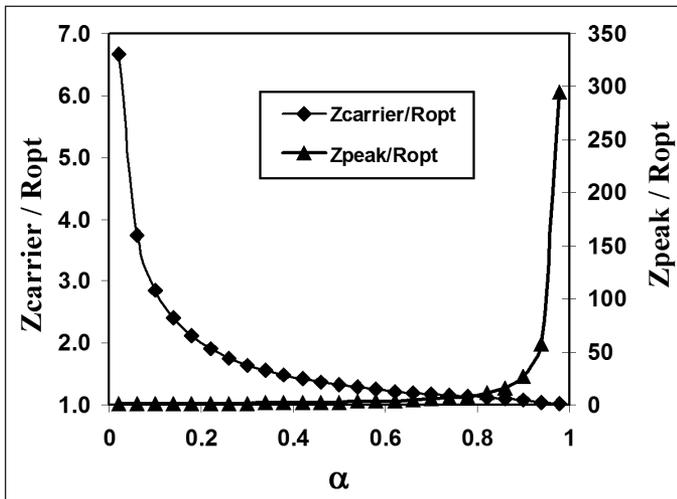Figure 5 shows the variation of the efficiency of the Doherty amplifier configurations at maximum drive

Figure 4 • Normalized impedances presented to the carrier and peak amplifiers at maximum drive level.
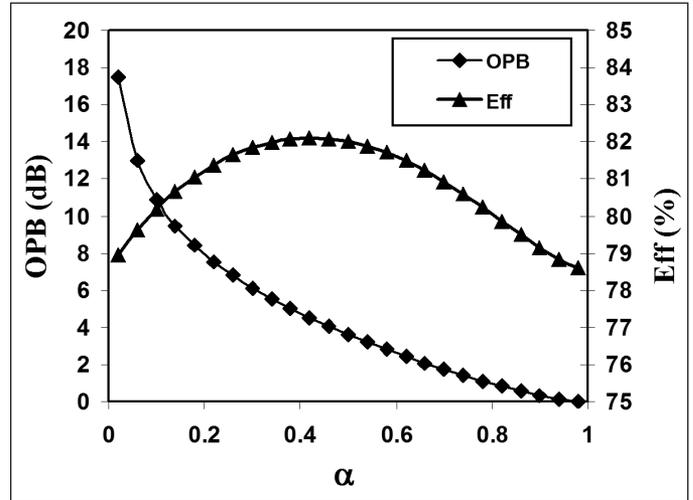

Figure 5 • Output power back-off and efficiency of the Doherty amplifier configurations at maximum drive level.

level. An efficiency of 82 .1 % can be achieved for $\alpha = 0.4$. At the extreme cases where $\alpha = 1$ or $\alpha = 0$, this efficiency is equal to that of a class B amplifier (78.5 %).

Figure 5 shows also a plot of the maximum output power back-off insuring a near peak efficiency versus α. An output power back-off of 7.95 dB is obtained with the configuration where $\alpha = 0.2$.

Implementation of Doherty Amplifier and Measurement Results

In order to assess the capabilities of the Doherty amplifier in providing high efficiency under output power back-off, a microwave integrated circuit (MIC)–type Doherty amplifier was implemented and characterized. The optimum load ($R_{opt} = 26\Omega$) of the *carrier* and *peak* amplifiers was determined from the dc characteristics of the GaAs FET device. The parameters of the designed Doherty amplifier configuration are given in Table 1. The values of R_L and Z_C were calculated using (3) and (6) and displayed in table I.

Parameter	Value
α	0.4
R_L	0.836 R_{opt}
Z_C	1.445 R_{opt}

Table I • Parameters of the Doherty amplifier configuration.

Circuit Design

The amplifier was designed at central frequency 1.9 GHz using Agilent-ADS. The *carrier* and *peak* amplifiers were designed using Fujitsu FLL107ME GaAs FET transistors on Duroid substrate, $\epsilon_r = 2.33$, H = 20 mils. During

operation of the Doherty amplifier, the carrier device is biased near pinch-off in class B (Vgs = -2.1 V, Vds = 6 V) whereas the *peak* device is biased below pinch-off in class C (Vgs = -2.4 V, Vds = 6 V). The output-matching network of the *carrier* amplifier was designed to present it with a load 5/2 times larger than its optimum (α=0.4). A quarter wave transmission-line at the fundamental frequency was used for short-circuit termination of second harmonic and also for the drain bias supply. The input-matching network was optimized to maximize the amplifier output-power and power-added efficiency. The gate bias was applied through a quarter-wave transmission line at 1.9 GHz. At the input of the Doherty amplifier, a standard broadband branch-line coupler was used as the quadrature input-hybrid network. At the output, the 50-Ohm load impedance is transformed to the desired optimum topology-load R_L with a quarter-wave transmission line.

Characterization and Linearization of the Doherty Amplifier Using a CDMA Signal

Using the measurement set-up illustrated in figure 6, the Doherty amplifier was first characterized using a CDMA2000 SR1 signal with a chip rate of 1.2288 Mcps and with a peak-to-average ratio of 5.5 dB. The characterization procedure in illustrated in the following steps:

- The input signal is generated using Agilent ADS software.
- The base-band waveforms are then downloaded into the signal generator (ESG 4438C).
- The ESG generates the corresponding RF input signal of the Doherty amplifier.
- A Performance Spectrum Analyzer (PSA E4446A) is used for high quality down-conversion of the Doherty amplifier output signal to an intermediate frequency (IF) (70 MHz).
- This IF signal is then fed to a single channel Vector Signal Analyzer (VSA 89600).
- Gain and delay adjustments are performed to get instantaneous complex envelops (I and Q components) both at the

input and the output of the power amplifier. These signals are then used to extract the complex gain of the power amplifier versus the input power.

Figure 7 shows the measured AM/AM and AM/PM curves after polynomial curve fitting. In these curves, the two typical compressions in the gain of the Doherty amplifier can be identified.

The predistortion function for the linearization of the Doherty amplifier was synthesized using the measured AM/AM and AM/PM characteristics. The resultant fully
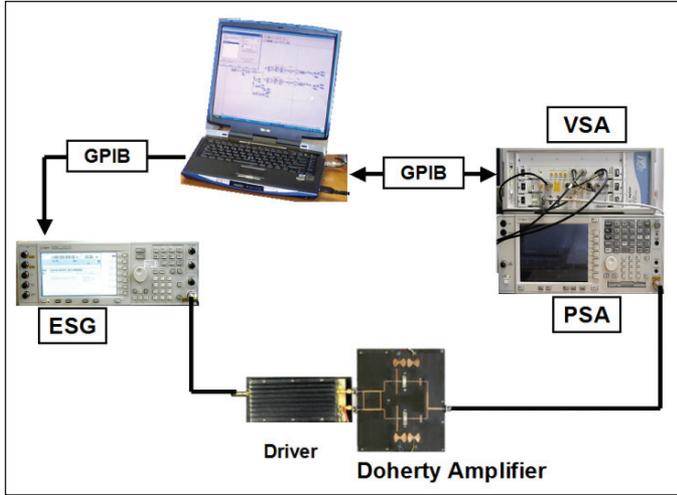
Figure 6 • Characterization set-up of the Doherty amplifier.

Figure 8 • Block diagram of the LUT based predistorter (10).

digital complex predistorter is implemented using Look-Up-Tables (LUT) [10].

Figure 8 shows the detailed block diagram of the LUT based predistorter. First, the components of the baseband signal (I and Q) are used to compute the squared magnitude of the input signal that indexes the LUTs containing the correction coefficients Ic and Qc. Second, these correction parameters are used to adjust the original signal components, I and Q, through a complex multiplication to obtain the predistorted Id and Qd components. These signals are digitally modulated and then up-converted to feed the Doherty amplifier.

Experimental Results

To evaluate the performance of the linearized Doherty amplifier in terms of the AM/AM and AM/PM characteristics linearity, the predistorter was added to the system
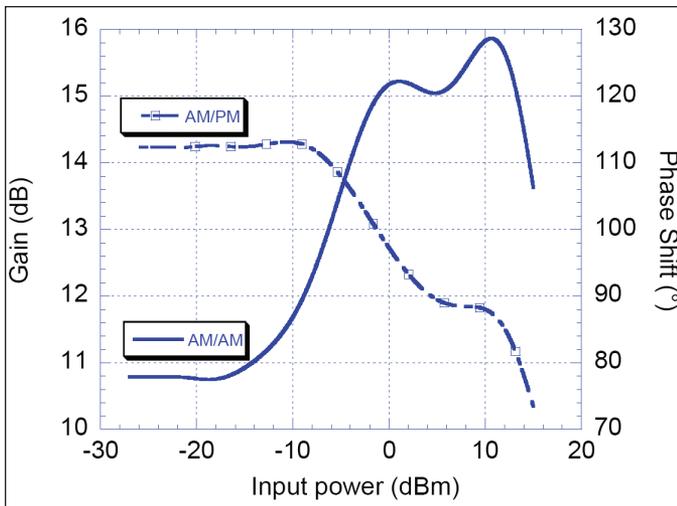
in figure 6 and the AM/AM and AM/PM curves were measured under the same CDMA2000 excitation. Figures 9 and 10 present the measured AM/AM and AM/PM characteristics with and without predistortion. A satisfactory improvement in the linearity of these characteristics has been obtained. The contributions of the predistorter to the efficiency and the linearity of the Doherty amplifier were also measured.

Figure 11 presents the measured ACPR for different output power levels. The ACPR was measured under a CDMA2000 excitation at an offset of 850 kHz from the carrier frequency. It can be observed that the ACPR improvement degrades as the output average power exceeds 25 dBm. This results from the clipping effects that occur at such power levels. The drain efficiency was also measured for the same output power range before and after the linearization of the Doherty amplifier. As shown in figure 12, the linearization process did not decrease the drain efficiency of the Doherty amplifier. Figure 13 presents the spectra measured at the output of
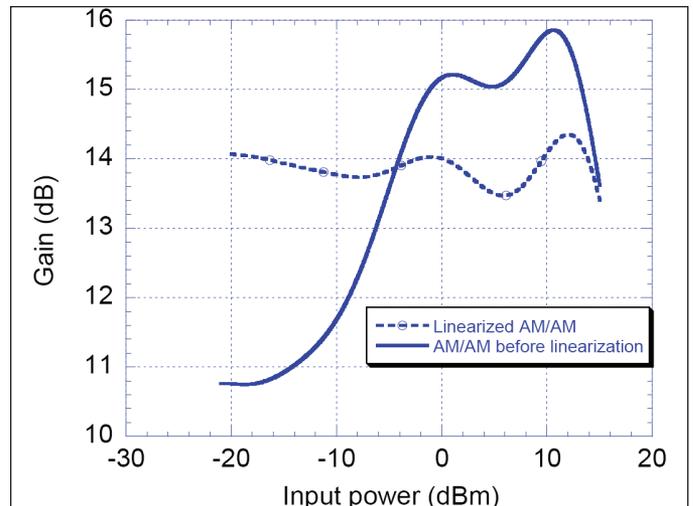

Figure 7 • Measured AM/AM and AM/PM characteristics of the Doherty amplifier.

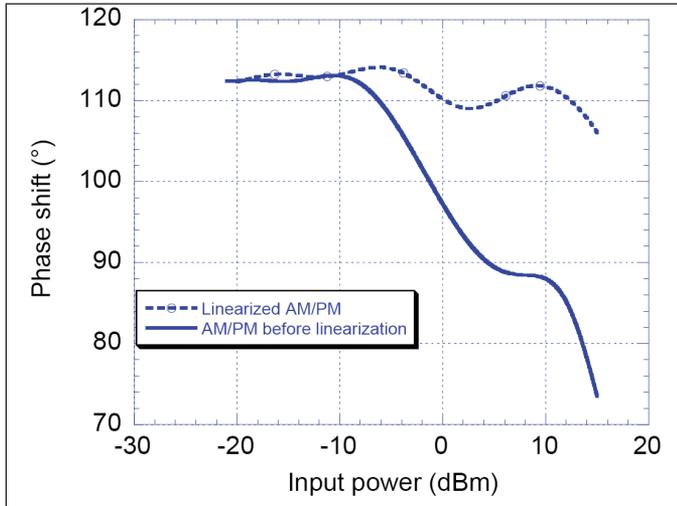**Figure 9 • Measured AM/AM curve after linearization.**

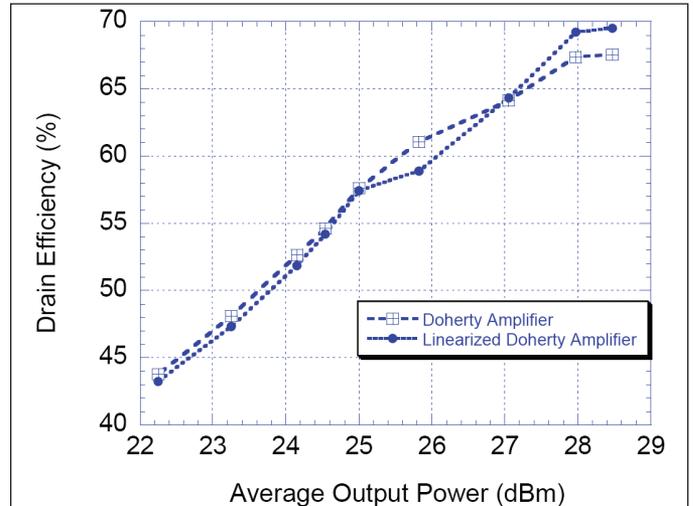Figure 10 • Measured AM/AM curve after linearization.

Figure 12 • Measured drain efficiency vs. average output power.

the Doherty amplifier before and after linearization. These spectra were obtained for an average output power of 25 dBm that corresponds to a drain efficiency of 55%.

Conclusion

An experimental realization at 1.9 GHz of a variable conduction angle Doherty amplifier was presented. Experimental validation of a fully digital complex base-band predistorter applied to the designed amplifier was carried using a CDMA2000 SR1 signal. An improvement of the Doherty amplifier linearity was obtained while maintaining its high power efficiency. At an output power back-off of 5.5 dB, the linearized amplifier has a power efficiency of 46% with an ACPR of 35 dBc.

Acknowledgment

This work was conducted among research activities of the author in PolyGRAMES research center (Ecole Polytechnique de Montreal, Canada). The author would like to thank Dr. Oualid Hammi for the technical support in the linearization of the fabricated amplifier.

About the Author

S. Bousnina received his Ph.D. in Electrical Engineering from the Ecole Polytechnique de Montreal, Montreal, Canada, in 2004. During his research stay at PolyGrames research center at the Ecole Polytechnique de Montreal, he conducted several research activities related to the characterization and modeling of active devices and design of the Doherty amplifier. From 2004 to 2005 he was an RF Development Engineer at Advanced Power Technology Solutions. In 2006 he joined M/A-COM Technology Solutions as Senior RF Design Engineer responsible for the design of high-power amplifiers for pulsed radar and general-purpose commercial applications.
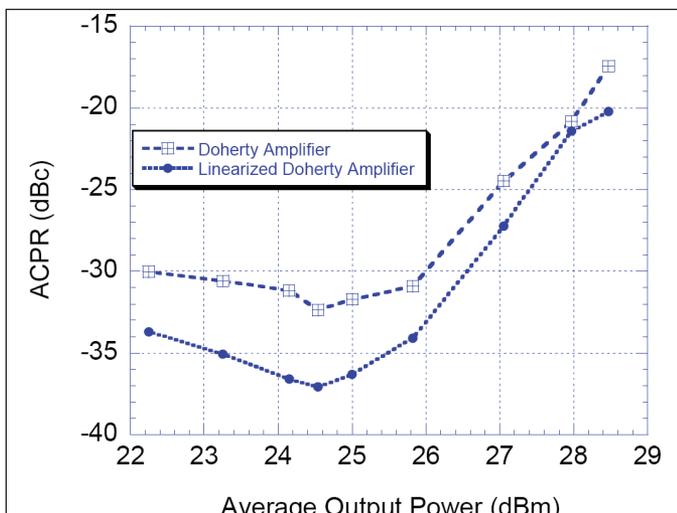

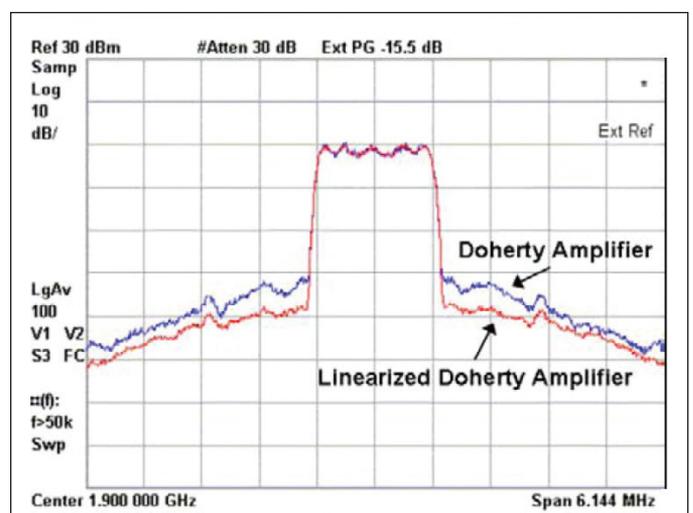Figure 11 • Measured ACPR vs. average output power.

Figure 13 • Output CDMA spectra of the Doherty amplifier before and after linearization.

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