A Multi-Channel Depth-Sounding Radar with an Improved Power Amplifier

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This article describes a research radar system, and the high linearity power amplifer techniques that enable accurate measurement of ice thickness

The Multi-Channel Coherent Radar Depth-Sounder (MCoRDS) system was developed by the Center for Remote Sensing of Ice Sheets (CReSIS) at the University of Kansas to map the thickness and underlying bed elevation for glaciers in Antarctica on the NASA Operation Ice Bridge (OIB) mission. Scientists believe that the lubricating effect of liquid water at the bed-ice interface will significantly increase the glacial flow resulting in more ice being discharged into the ocean. Bed elevation that is below sea level is particularly susceptible to this effect. Therefore, to better predict the future movement of ice sheets in Antarctica, scientists and modellers need to know the current elevations and topography of the bed beneath several outlet glaciers in Antarctica. The MCoRDS system, flown on the NASA DC-8, was designed to sound these glaciers capturing the surface and bed echoes from both low and high altitude flights. The ice thickness can be obtained from these measurements and, in conjunction with altimeter data, the bed elevation can be determined allowing modellers and scientists to better understand the current status of these glaciers, as well as, identifying those at risk of increasing in velocity.

MCoRDS System Design

MCoRDS is the latest radar depth-sounding system in a long line of airborne radars developed at the University of Kansas [1, 2]. It is a chirp-pulsed radar system using a 1- to 10-µs pulse that operates at a 193.9 MHz center frequency with a 9.5 MHz bandwidth. Transmission and reception take place using a 5-element antenna array mounted on the bottom of the DC-8 aircraft. This array is housed in a customized antenna fairing designed by KU's Aerospace Engineering Department. During transmission, each of the five antennas is driven by a unique waveform digitally produced from a custom multi-channel waveform generator allowing the operator to adjust the timing, frequency, phase, and amplitude of each transmit waveform. This capability enables control of the transmitted radiation pattern, time side-lobe management techniques, and implementation of 0/π modulation to further reduce coherent noise and increase the system's signal-to-noise ratio (SNR) [3]. Each transmit channel has the capacity to output 100 W (50 dBm) of power for a peak transmit power of 500 W. Lastly, special precautions were taken during the radar design phase to reduce the
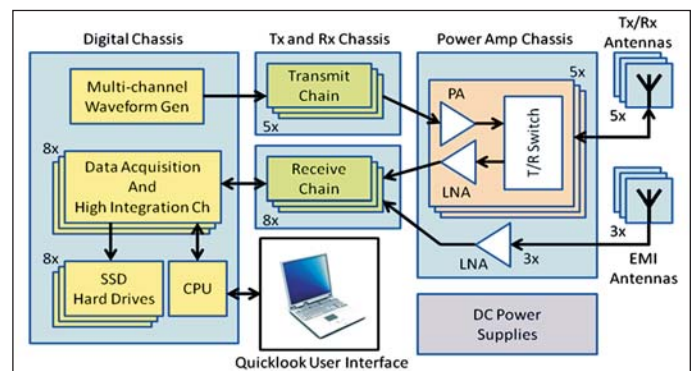

Figure 1 · High-level block diagram of MCoRDS.

Figure 2 · Custom eight-channel waveform generator photo.

Figure 3 · Strong surface echo from the 1-μs waveform collected during a low-altitude survey of the Thwaites outlet glacier in Antarctica.

Figure 4 · Strong bed echo from the 10-μs waveform collected during a low-altitude survey of the Thwaites outlet glacier in Antarctica.

effects of both internal and external electromagnetic interference (EMI) which includes customized chassis, fiber-optic controls, and EMI monitoring antennas within the cabin.

Multi-Channel Waveform Generator

An eight-channel direct-digital synthesizer (DDS) was developed by CReSIS, as seen in Figure 2, to enable digital beam steering of the transmitted waveform, as well as, to apply digital predistortion linearization. Built around the AD9910 DDS chip, the eight-channel waveform generator enables the illuminating radiation pattern to be digitally modified on a pulse-to-pulse basis if desired. Two key benefits of this capability include improved surface clutter suppression and more efficient off-nadir illumination for side-looking imaging of the ice-bed interface [4].

Power Amplifier Chassis

The power amplifier (PA) used in MCoRDS for the DC-8 mission was a custom designed 150 W module from Polyfet RF Devices. The PA was operated at 100 W and pulsed as close as possible to the RF transmit pulse where the rise and fall time of the PA was measured to be 1 μs and 3 μs, respectively. In order to transmit a 1 μs pulse successfully, changes to the transmit timing had to be made due to the long rise and fall times.

DC-8 Mission Measurements

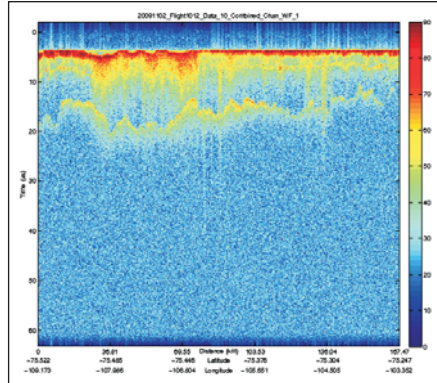For the low-altitude flights (nominally 500 meters above the ground),

MCoRDS was setup to transmit a 1 μs duration pulse to capture the surface echo and followed by sixteen 10-μs pulses (integrated in hardware) to capture the bed echo. Using preliminary data processing results, the performance of the MCoRDS system was monitored continuously throughout the campaign. Figures 3 and 4 show a sample of the results, which were produced in the field within 24 hours of collecting data. These echograms show surface and bed echoes from a low-altitude Thwaites outlet glacier flight with SNRs exceeding 40 dB.

New PA Design and Linearization

For depth sounding applications, the transmitter PA needs to be linear to reduce the side-lobe levels of the transmitted pulse. The CReSIS depth sounding radars use a pulse compressed, linear frequency modulated (FM) chirp signal with a pulse width between 1 and 10 μs, which, when transmitted with low time-bandwidth products creates mid-band ripples in the amplitude spectrum [5]. The mid-band ripples, known as Fresnel ripples, create range side-lobes which are typically reduced by applying an amplitude tapering function, typically a Tukey window. However, the efficiency of the windowing is based on the concept of
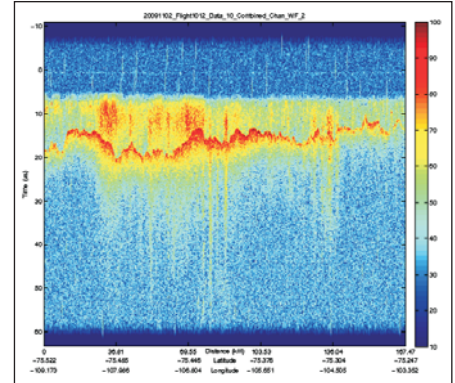
shaping a perfectly rectangular spectrum; thus, range side-lobes will be generated when there are deviations from the ideal spectrum amplitude and quadratic phase [6]. These range side-lobes can mask weak returns which could represent internal layers or surface clutter depending on the application.

A new 100 W PA module prototype, shown in Figure 5, was designed to operate from 180 to 210 MHz with higher efficiency, faster switching speeds, improved linearity and a lighter, more compact design. The PA is a 3-stage design using the SP202, SP203 and SD703 transistors from Polyfet, as depicted in Figure 6. The PA switching, shown in Figure 7, is
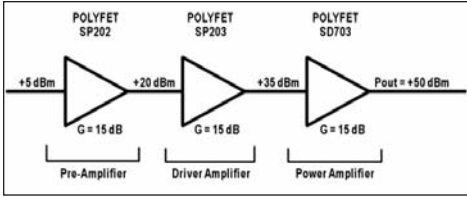

Figure 5 · New power amplifier module prototype.

Figure 6 · New power amplifier block diagram.

Figure 7 · New power amplifier switching circuit

accomplished by applying the modified high-speed pulsing circuit of [7] to the gate bias circuitry of each transistor. Modifications were made in order to reduce the charging time of the large capacitors required in the RC drain-to-gate stability network for the SP202 and SP203 transistors.

High-Speed Switching Circuit Design

Typically, the gate bias voltage (V_{GS}) is switched to remove the bias current; however, this requires a large current to be driven into the gate in order to charge the large input gate capacitance (C_{GS}) as well as the Miller capacitance (C_{GD}) of the FET. Figure 8 illustrates the MOSFET equivalent circuit with only those parasitic components that have the greatest effect on switching. L_D and L_S are the drain and source inductances, respectively, and typically are around a few tens of nH [8]. Furthermore, Figure 8 shows the drain-to-gate feedback stability network (R_{FB} and C_{FB}) needed for the SP202 and SP203 transistors. Once C_{GS} is fully charged, the drive current starts to charge the Miller capacitance (C_{GD}) which requires a longer charge time than that for C_{GS}. These charge times result in a turn-on and turn-off delay of the transistor. The turn-on charging waveforms are illustrated in Figure 9, where turn-on delay is t_3 [8]. The RC feedback stability network further increases the charge time (i.e. turn-on delay).

The high-speed switching circuit operation is given in Figure 10. Q1 through Q3 is a TTL level drive circuit for fast switching of Q4. R1 controls the operating drive current of the circ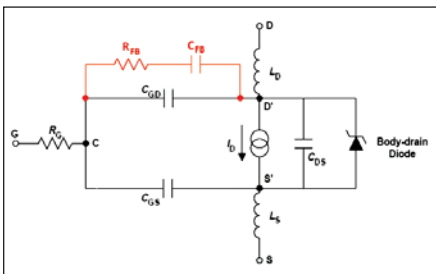uit with smaller values of R1 providing higher current which result in faster switching speeds, but also increased power dissipation. When the switching circuit is turned on, Cgs(Q4) is charged along the red, solid current line according to Equation (1) [7].

$$T\_charge = Rds(on,Q2) * Cgs(Q4) \qquad (1)$$

Rds (on,Q2) is the "on" state drain-source resistance of Q2 and Cgs(Q4) is the gate-source capacitance of Q4. When the switching circuit is turned off, Cgs(Q4) is discharged along the blue, dotted line according to Equation (2) with Q3 acting as a voltage controlled variable resistor [7].

$$T\_discharge = Rds(Q3) * Cgs(Q4) \qquad (2)$$

Rds(Q3) is the voltage controlled variable resistance of Q3. A BJT, rather than a FET, is used for Q3 to reduce the fall time due to the lower input threshold voltage of Q3 which maintains a lower Rds(Q3) while Cgs(Q4) is discharged [7]. Also, since Q4 has a maximum V_{GS} of ±20 V, the switching circuit requires a zener diode, as shown in Figure 7, to protect Q4 from the +28 V supply voltage. The breakdown voltage of the zener diode is selected according to Equation (3) [7].

$$\left|V_{gs(th)} \text{ of } Q4\right| < \left|V_{BR,Zener} - V_{CC}\right| < \left|Maximum V_{gs} \text{ of } Q4\right| \qquad (3)$$

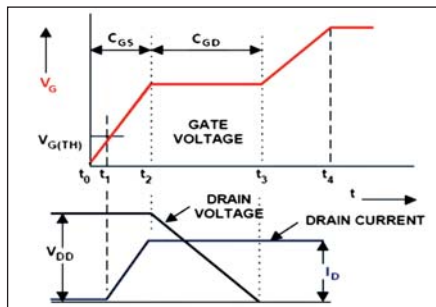Figure 8 · MOSFET equivalent circuit with RC drain-to-gate feedback.

Figure 9 · Gate and drain charging waveforms (8).

Figure 10 · Operation of high-speed switching circuit (7).

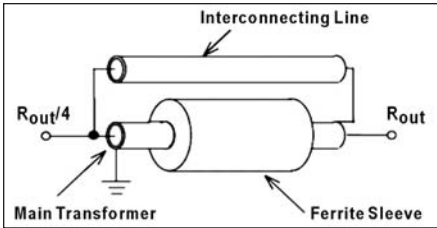**Figure 11** · **1:4 ED Unun transformer diagram (10).**

	Input Matching Network	Output Matching Network
SP202	4:1 Equal Delay Unun	1:4 Equal Delay Unun
SP203	4:1 Equal Delay Unun	1:4 Equal Delay Unun
SD703	1:1 Balun w/ 4:1 Balbal	1:9 Balbal w/ 1:1 Balun

Table 1 · **Impedance matching / transformers / baluns.**

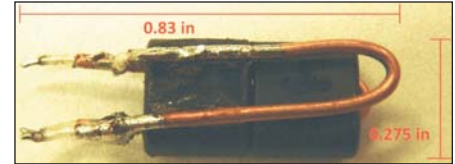**Figure 12** · **1:4 ED Unun transformer implementation—straight.**

Figure 13 · **1:4 ED Unun transformer implementation—bent.**

It can be seen from Equations (1) and (2) that the FETs and BJT selected should have low Rds(on) and low Cgs for faster switching. Figure 7 indicates the components selected for implementing the switching circuit.

Matching Network Design

In the design of RF power amplifiers, wideband transformers play an important role in the quality of the amplifier as they are a fundamental component in determining the input and output impedances, gain flatness, linearity, power efficiency, and other performance characteristics. Selection of the magnetic materials, the conductors, and the method of construction is crucial as these choices are significant in determining the overall performance of the transformer. The theory and approach in [9] was used to design, simulate, and construct the transformers used in the matching networks. Three different configurations of impedance transformers were utilized in the matching networks as outlined in Table 1.

The 1:4 Equal Delay (ED) Unun transformer, depicted in Figure 11, is a modification of the basic 1:4 Ruthroff transformer. No ferrite loading is required for the added interconnecting delay line. Also, there is no voltage drop on the outer conductor, thus no isolation is required from one end to the other [10]. Typically, the best response is achieved when the ED transformer is constructed using a straight, coaxial cable loaded with cylindrical cores or stacked toroids so that the opposite ends of

the transformer can be separated by the length of the transmission lines. However, due to layout constraints of the T/R module, the ED transformer was also constructed using a bent coaxial cable loaded with ferrite so that it could be mounted vertically and conserve horizontal real estate on the board layout. Furthermore, the 1:4 ED transformer was used in reverse to realize the 4:1 ED transformers. The straight and bent ED transformer implementations are shown in Figure 12 and Figure 13, respectively. The geometric mean is used to determine the optimum characteristic impedance (Z_0) of the coaxial cable according to Equation (4).

$$Z_0 = \sqrt{Z_{in}Z_{out}} \tag{4}$$

Thus, for both ED transformers a 25 Ω coax (Micro-Coax UT-047-25) was used to construct both the straight and bent versions. Five, 43 material ferrite beads (Amidon FB-43-101) were used for the straight
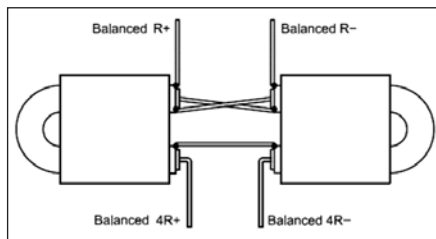

Figure 14 · **4:1 Balbal transformer diagram (9).**

version, while two 43 material ferrite binocular cores (Amidon BN-43-2302) were used for the bent version.

The 4:1 Balbal transformer was constructed according to the diagram and implementation shown in Figure 14 and Figure 15, respectively. The optimum Z_0 of 25 Ω was calculated using Equation (4) and the same 25 Ω coax (UT-047-25) and two, 43 material binocular cores (BN-43-2302) were used to construct the 4:1 Balbal. Typically, this 4:1 transformer is implemented in a horizontally planar fashion, as depicted in Figure 14, but to save horizontal real estate on the board layout the transformer was implemented vertically instead with no change in performance.
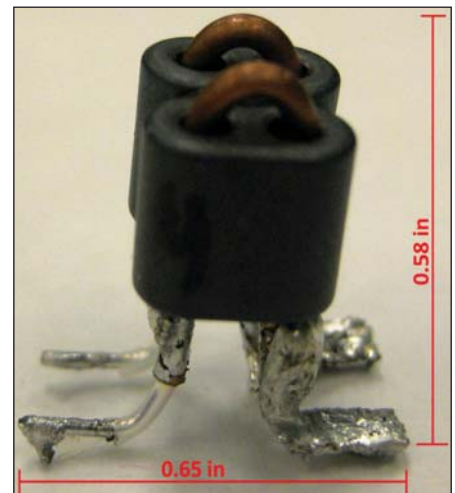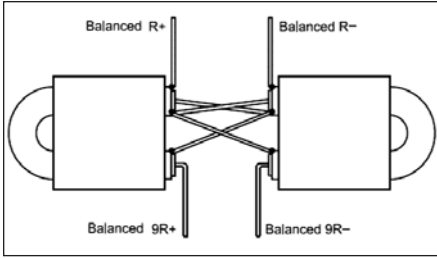

Figure 15 · **4:1 Balbal transformer implementation.**

Figure 16 · 1:9 Balbal transformer diagram (9).

Freq. [MHz]	Gain [dB]	Efficiency [%]	2nd Harm. [dBc]	3rd Harm. [dBc]
180	46.3	40	-34	-33
190	46.8	50	-35	-33
200	46.5	53	-33	-29
210	45.7	56	-33	-32

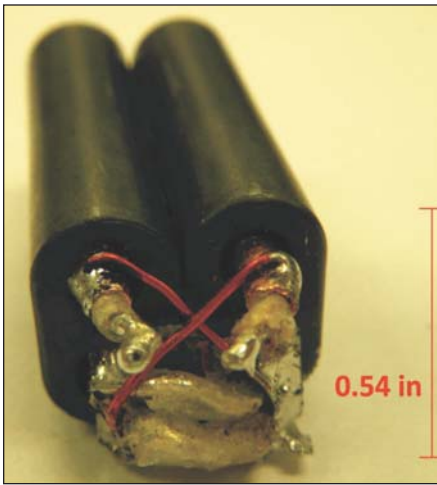**Table 2 · New PA gain and efficiency, plus 2nd and 3rd harmonic level measurements.**

Figure 17 · 1:9 Balbal transformer implementation.

The 1:9 Balbal transformer was constructed according to the diagram and implementation shown in Figure 16 and Figure 17, respectively. The optimum Z_0 of 16.7 Ω was calculated using Equation (4) and 15 Ω coax (Micro-Coax UT-085C-15) along with two, 43 material binocular cores (Amidon BN-43-6802) were used to construct the 1:9 Balbal transformer. Typically, this 1:9 transformer is implemented in a horizontally planar fashion, as depicted in Figure 16. However, to conserve board layout space the transformer "halves" were stacked together and laid out horizontally, as shown in Figure 17. Since the 1:9 Balbal is responsible for the most crucial transformation of the design (i.e., the final output stage), the longer cores and cables were used to increase the performance of the transformer [9]. As a final note, 61 or 64 material could also be used for this design as they have characteristics similar to 43 material beyond 100 MHz.

After constructing each transformer, 1-port *S*-parameters were taken using the HP8722D Vector Network Analyzer (VNA) with the transformer terminated in 50 Ω. Then, two identical transformers were connected back-to-back and 2-port *S*-parameters were measured using the same VNA. A MATLAB script was used to retrieve the data via the GPIB port using a labtop computer and convert the .DAT files into .S1P and .S2P files. The *S*-parameters (in the form of .S1P and .S2P files) were then introduced into Advanced Design System (ADS) 2008 Version 2 to create lumped element equivalent circuit models for each transformer based on the equivalent circuit model in [9]. The equivalent circuit models for each transformer were then used in the PA design simulation instead of the ADS component XFERTL2, to provide a more accurate representation of the parasitic reactive elements of each transformer. The ADS equivalent circuit model for the 1:9 Balbal transformer is provided in Figure 18.

Table 2 provides the continuous-wave (CW) gain, efficiency, and 2nd and 3rd harmonic levels across the operating band at 10 MHz intervals. The rise and fall time are given in

Rise Time [ns]	Fall Time [ns]
391	79.1

Table 3 · New PA rise and fall time measurement.

Table 3 for a 10 µs pulse with a 1 kHz pulse repetition frequency (PRF). The PA prototype enclosure measures 4" × 4" × 1" and weighs 16 ounces.

Digital Predistortion Linearization

The setup of Figure 19 was used to test the digital predistortion amplitude correction for the new PA. A 10 µs pulse with Tukey tapering on transmit and double-Blackmann (Blackmann[2]) filtering on receive was measured and then corrected using amplitude predistortion only. Figure 20 shows a simulated ideal transmit pulse (blue) along with the measured PA transmit pulse with Tukey tapering only (red) and with amplitude predistortion (green), which included Tukey tapering. Assuming the return signals will be attenuated versions of the PA transmitted pulse of Figure 20, a strong return (representing the bedrock, in red) and a delayed weak return (representing an internal layer, in green) were simulated and filtered using a Blackmann[2] window. The delayed weak return was assumed to have amplitude of –55 dB relative to the bedrock return.

Figure 21 shows the pulse compression response of the 10 µs pulse with Tukey tapering only. Figure 22 shows the pulse compressed response of the 10 µs pulse with amplitude predistortion correction, which includes Tukey tapering.

Comparing the side-lobe levels of Figure 21 and 22, Table 4 provides the approximated side-lobe level reduction improvement of the amplitude predistortion based on the time range.

Time Range [μs]	Side-lobe Level Improvement [dB]
-10 to -5	~17
-5 to 0	~ 10
0 to 5	~1
5 to 10	~6

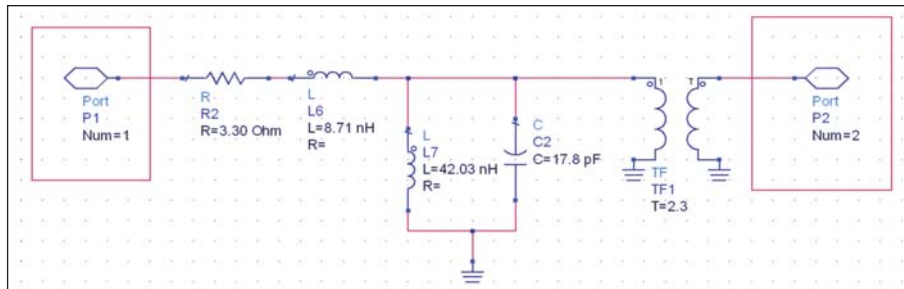Table 4 · Pulse compression side-lobe improvement.

Figure 18 · 1:9 Balbal ADS equivalent circuit model.

Conclusions

An eight-channel DDS was developed by CReSIS to enable digital beam steering of the transmitted waveform, as well as, to apply digital predistortion linearization. Echograms from flight data of MCoRDS using the current PAs show surface and bed echoes from a low-altitude Thwaites outlet glacier flight with SNRs exceeding 40 dB. To improve the measurement results of MCoRDS, a high-speed, pulsed, VHF power amplifier was developed and linearized using amplitude predistortion to obtain high linearity and high efficiency. Also, the faster switching speeds will improve the SNR by allowing the receiver to acquire more of the surface clutter returns.

The frequency response of the new PA was 140 to 210 MHz with 70 MHz bandwidth and PAE ranging from 25 to 56%. The switching circuit reduced average current consumption to 117 mA (or 3.28 W at +28 V) for a 10 μs, 1 kHz PRF pulse at maximum output power with a rise time of 391ns and a fall time of 79.1 ns. The amplitude predistortion decreased far range side-lobe levels below −57 dBc, with a maximum reduction of 17 dB over the Tukey (transmit) and Blackmann[2] (receive) windowing alone.
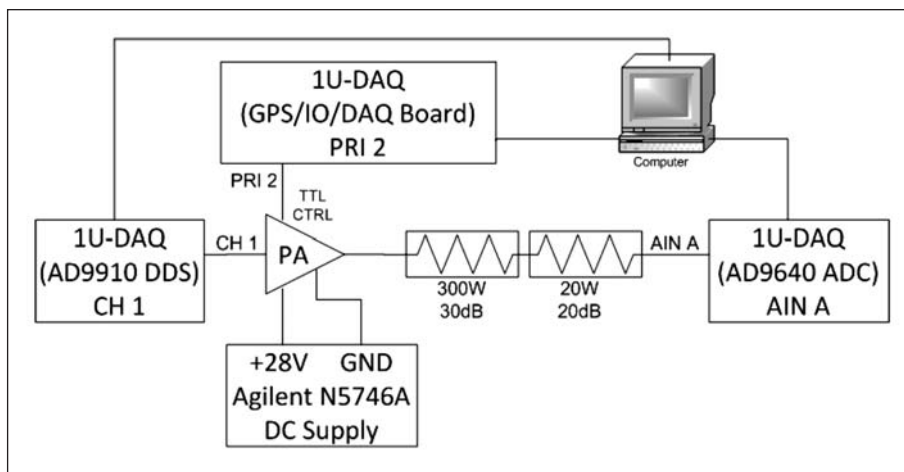
Acknowledgment

Figure 19 · Digital predistortion linearization block diagram.

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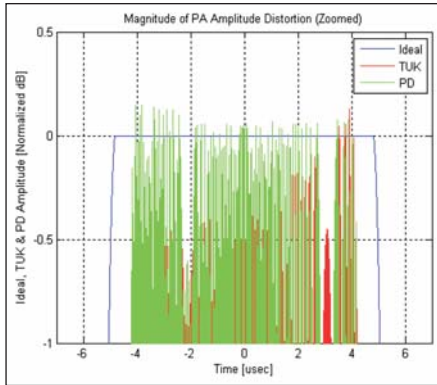
Figure 20 · Comparison of transmit pulse: Ideal, Tukey weighting only, and amplitude predistortion.
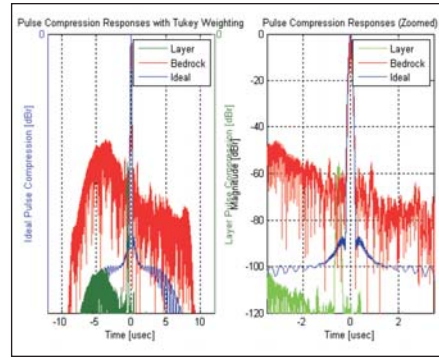

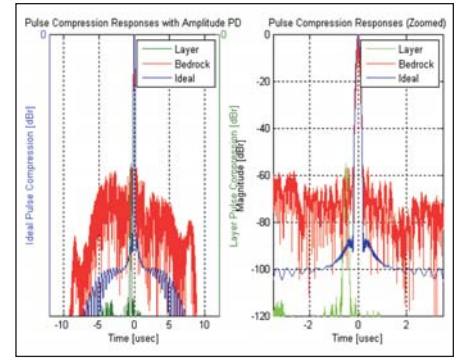Figure 21 · Pulse compressed response without amplitude predistortion (Tukey weighting only).

Figure 22 · Pulse compressed response with amplitude predistortion.

Author Information

Kevin Player received his BSEE and MSEE degree from the University of Kansas in 2007 and 2010, respectively. From 2007 to 2010, he worked as a graduate research assistant for the Center for Remote Sensing of Ice Sheets (CReSIS) designing power amplifiers and other RF hardware for radars used in remote sensing applications. In 2009, he was selected to be the 1st Engineering student from the University of Kansas to study and perform research at the Indian Institute of Technology in Kanpur, India where he worked on developing the new UAV power amplifier module and a Ku-band phased-array microstrip antenna. Presently, he is working as a Radar Systems Engineer at JT3, LLC in Las Vegas, NV. He can be contacted at playerk@ cresis.ku.edu.

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